Rejection - 35 U.S.C. § 112, first paragraph:

Claims 151-174 and 176-186 have been rejected under 35 U.S.C. §112, first paragraph, in that Applicants failed to provide an adequate written description of how the memory controller provides block size information to the memory device. Applicants respectfully disagree.

The specification of the above-referenced application describes a method of controlling a memory device by a memory controller. (See, for example, page 13, lines 13-17). In one embodiment, this method of controlling includes providing block size information to the memory device wherein the block size information is representative of an amount of data to be input by the memory device. (See, page 22, lines 7-10 ("The last byte contains ... BlockSize [0:3] ...."); page 27, lines 23-30 (the block size information "specifies the size of the data block transfer"); and page 20, line 23 to page 21, line 1, (the memory device "... accept[s] data from the master (in the case of a write request) in a data block transfer."); in addition, see page 74, lines 1-31).

One type of encoding scheme for the block size is described on page 27, line 24 to page 28, line 11 of the specification. In this regard, the application states:

> Blocksize[0:3] specifies the size of the data block transfer. If BlockSize[0] is 0, the remaining bits are the binary representation of the block size (0-7). If BlockSize[0] is 1, then the remaining bits give the block size as a binary power of 2, from 8 to 1024. A zero-length block can be interpreted as a special command, for example,

to refresh a DRAM without returning any data, or to change
the DRAM from page mode to normal access mode or vice-versa.
(page 27, lines 23-30).

The applications notes, however, that " [p]ersons skilled in the art will recognize that other block size encoding schemes or values can be used." (page 28, lines 13-14).

Thus, Applicants respectfully submit that the application, as filed, provides an adequate written description of how a controller or master controls a memory device, in connection with a write operation, via providing block size information to the memory device.

Rejection - 35 U.S.C. §102(b):

The pending rejection under 102(b), in view of the '459 application, is substantively identical to the rejection set forth in the Office Action dated August 1, 2000, wherein the Examiner rejected the then pending claims, under 35 U.S.C. §102(b), based on the '459 Application. This rejection was addressed in the Amendment dated October 31, 2000. The rejection was believed to be overcome, as demonstrated by the Notice of Allowance mailed November 28, 2000.[1]

It is respectfully submitted that the '459 Application does not anticipate claims 151-153, 156, 159-162, 166-167, 171-172, 174, 178,

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[1]By way of note, in a telephone interview on November 21, 2000, the Examiner expressed a concern that claim 151 could be interpreted in such a way as to read on the '459 Application. Applicants submitted an Amendment on November 22, 2000 to address the Examiner's concern. A Notice of Allowance was mailed on November 28, 2000.

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180, 182-184, and 186.[2] In this regard, memory 1 disclosed in the '459

Application -- unlike the claimed invention -- is _not_ provided nor does

it receive information indicating the "number of words to transfer"[3] as

required by the claims of the instant application. For example, claim

161 recites in pertinent part:

> A method of operation in a synchronous memory device, ...
> the method of operation of the memory device comprises:
>   receiving first block size information from a memory
> controller, wherein the first block size information
> represents a first amount of data to be input by the memory
> device in response to an operation code;

The memory in the '459 Application does not receive block size

information. Rather, memory 1 of the '459 Application responds to the

sequentially applied address and control signals from the memory

control device 2 in order to store the appropriate number of words.

It is the memory control device 2 of the '459 Application which

receives, decodes and stores the information indicating the number of

words to be stored in memory 1. The memory control device 2 stores the

number of words in a counter, and, based thereon, generates and

sequentially applies the appropriate address and control signals

necessary to write the words to memory 1. The information indicating

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[2]The discussion below is very similar to the discussion set forth
in the October 31, 2000 Amendment.

[3]For the purposes of this discussion, the phrase "number of words
to transfer" may be assumed to correspond to "block size information".

the number of words to transfer is <u>not</u> provided to memory 1 (and as such, memory 1 does not receive such information).

The '459 Application

The '459 Application discloses a system including memory 1, memory control device 2, cache memory 3, a main processing device 4, and an input/output processing device 5. (See Figure 2). The memory 1 is connected to memory control device 2 via memory bus 6. Memory control device 2 and input/output processing device 5 are both connected to bus 7 (See, the '459 Application, page 3 lines 11-16, and Figure 2).

Communication between memory 1 and devices connected to bus 7 is executed via memory control device 2. In this regard, the '459 Application states that "control of reading or writing from memory 1 is performed by memory control device 2 via memory bus 6." (page 3, line 13-14). The memory control device 2 controls memory 1 via a memory interface which includes memory address signal 242, memory data [bus] 243 and memory response signal 240. (See, the '459 Application, page 6, lines 17-21). Address signal 242 and data 243 are employed to transfer address and data, respectively, between memory control device 2 and memory 1. (See, the '459 Application, page 6 lines 18-21 and Figure 6).

In operation, a "number of words to transfer," together with origin and destination addresses, are provided to memory control device 2. (See, e.g., the '459 Application, page 4, lines 36-39). Memory control device 2 increments or decrements source and destination

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address counters while maintaining a count of the number of remaining words to be transferred to memory 1. In this regard, the '459 Application, on page 5, lines 21-24 states:

> The counter for the remaining number of words to transfer, which is set with number of words to transfer, is decremented each time data is transferred and stored, and when that count value reaches zero, transfer ... ends.

The memory control device 2 of the '459 Application, at all times, maintains the information regarding the number of words to transfer, generates the appropriate control and address signals, and applies the control and address signals which are necessary to transfer the requested number of words to memory 1. (See, the '459 Application, page 7, lines 26-39, and Figure 9). The memory control device 2 receives, decodes and stores, in a counter 203, information indicating the number of words to transfer to memory 1 and, based thereon generates address and control signals and sequentially applies those addresses and control signals in order to transfer the indicated number of words from memory 1. The memory control device 2 does <u>not</u> provide information indicating the number of words to transfer to memory 1.

Although the '459 Application does not describe memory 1 in great detail,[4] memory 1 is most likely a standard off-the-shelf memory device or memory module incorporating the same, for example, memory devices

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[4] The '459 Application suggests the use of "The latest dynamic RAMs" featuring "Nibble Mode Support" as in "*Nikkei Electronics*, April 1983." (see page 8, lines 38-39).

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like those described in the Kung et al., U.S. Pat. 4,449,207, and Voss, U.S. Pat. 4,646,270. The memory 1 described in the '459 Application does not appear to input or output data synchronously with respect to a clock signal. Instead, control signals such as function signal 241 and memory response signal 240, generated by memory control device 2, are employed to signal the transfer of data between memory 1 and memory control device 2. (See, the '459 Application, Figure 9, and page 7, lines 26-34). The writing of data to memory 1 from memory control device 2 is described on page 7, lines 31-34 as follows:

> ...after response 240 is acquired, if memory function signal 241 is made the write mode [ ] the contents of transfer destination address counter 203 are output as memory address signal 242, memory data 243 is transferred to and stored at the transfer destination memory area."

The '459 App. Does Not Anticipate Claims 151-153, 156, 159, 178, and 180

Claim 151 is directed to a method of controlling a memory device and requires, among other things, providing first block size information to the memory device. The first block size information is representative of a first amount of data to be input by the memory device in response to an operation code.

As mentioned above, information indicating the number of words to be transferred by the memory control device 2 is not provided to memory 1. Instead, memory control device 2 of the '459 Application receives, decodes and stores that information in a counter, and, based thereon,

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sequentially generates the address and control signals necessary to write the words to the memory device. In this regard, the system described in the '459 Application is similar to the system described in Jackson, U.S. Pat. 4,315,308[5]. The claims of the parent (i.e., App. Ser. No. 09/252,997, now, U.S. Pat. 6,034,918) of the instant application were initially rejected as being anticipated by Jackson but ultimately found patentable over Jackson.

Importantly, memory 1 of the '459 Application does not receive information indicating the number of words to be transferred. The memory 1 simply responds to the sequentially applied address and control signals provided by memory control device 2.

Thus, for <u>at least</u> these reasons, the '459 Application does not anticipate claim 151 or the claims which depend therefrom.[6]

<u>The '459 App. Does Not Anticipate Claims 161, 162, and 166-167, and 182-184</u>

Claim 161 is directed to a method of operation in a memory device, and, like claim 151, requires that the memory device <u>receive</u> first block size information <u>from</u> a memory controller.

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[5] Jackson, U.S. Patent 4,315,308, formed the basis of the 35 U.S.C. §102(b) rejection made in the parent application (App. Ser. No. 09/252,997, now, U.S. Patent 6,034,918) It was previously noted that the '459 Application is similar in many respects to Jackson.

[6] It should be noted that claim 152 requires that the memory device inputs the first amount of data synchronously with respect to an external clock signal. The memory disclosed in the '459 Application does not input data in this manner.

For reasons similar to those mentioned above, the memory disclosed in the '459 Application does not receive the information indicating the number of words to be transferred. The memory of the '459 Application simply responds to the sequentially applied address and control signals from the memory control device 2. The memory control device 2 receives, decodes and stores information that indicates the number of words to be transferred to memory 1 in a counter, and, based thereon, generates and sequentially applies the appropriate address and control signals necessary to write the appropriate number of words to memory 1. The information indicating the number of words to be transferred is <u>not</u> provided to memory 1.

Thus, for <u>at least</u> these reasons, the '459 Application does not anticipate claim 161 or the claims which depend therefrom.

The '459 App. Does Not Anticipate Claims 171-172, 174 and 186

Claim 171 is directed to a method of operation of an integrated circuit, wherein the integrated circuit includes a dynamic random access memory array. Claim 171 requires, among other things, that the integrated circuit <u>receive</u> block size information. The memory device disclosed in the '459 Application does <u>not</u> receive the information indicating the number of words to transfer. Thus, for <u>at least</u> this reason, the '459 Application does not anticipate claim 171 or its dependent claims.

Information Disclosure Statement

Applicants submit concurrently herewith an Information Disclosure Statement (IDS) and accompanying Form PTO-1449, identifying two (2) references, namely U.S. Patent 5,034,964 and Japanese Patent Application No. S62-51509, that were both identified in previous IDS submissions, but were not clearly noted (by way of, for example, the Examiner's initials) by the Examiner as being formally considered. For the convenience of the Examiner, a copy of the Form PTO-1449 identifying each reference is attached. It is respectfully requested that the Examiner make his consideration of these references clearly and formally of record with the next Action.

CONCLUSION

Applicants request entry of the foregoing Amendment. Applicants submit that all of the claims present patentable subject matter. Accordingly, allowance of all of the claims is respectfully requested.

It is noted that should a telephone interview expedite the prosecution in any way, the Examiner is invited to contact Neil Steinberg at 650-947-5325.

Respectfully submitted,

Date: May 31, 2001

Neil A. Steinberg
Reg. No. 34,735
650-947-5325